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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,760	03/15/2004	Jozef C. Mitros	TI-35141.1	3452

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EXAMINER	
DOAN, THERESA T	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,760	MITROS ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendments to the Specification that filed on 03/15/04 are acknowledged and entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10-11, 13, 15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushita (U.S Pat. 5,502,321).

Regarding claims 10 and 13, Matsushita (figures 1-13) discloses a method of manufacturing a semiconductor device, comprising:

implanting source region (10,12) and drain region 11 having similar (N-type) doping profiles (see Figure 1, column 7, lines 50-53 and column 13, lines 55-59) in a semiconductor substrate 1 (column 13, lines 48-50) , thereby defining a channel region 4 (column 13, line 51) extending from the source region (10,12) to the drain region 11 (see figure 1);

locating a dielectric layer (5,6) over the source and drain regions (see figure 1), the dielectric layer (5,6) having a first thickness 5 (or 34) of about 15 to 20 nm (column 17, lines 27-28) and a second thickness 6 (or 33) of about 10 nm (column 17, lines 23-

24), wherein the second thickness 6 is substantially less than the first thickness 5 and is partially located over the channel region (see figure 13 and column 18, lines 31-40); and

forming a gate 7 (figure 1) or 35 (figure 13) over the dielectric layer (5,6) (column 17, lines 55-59), wherein the second thickness 6 is located between an end of the gate 7 and one of the source and drain regions (10,12).

FIG. 1

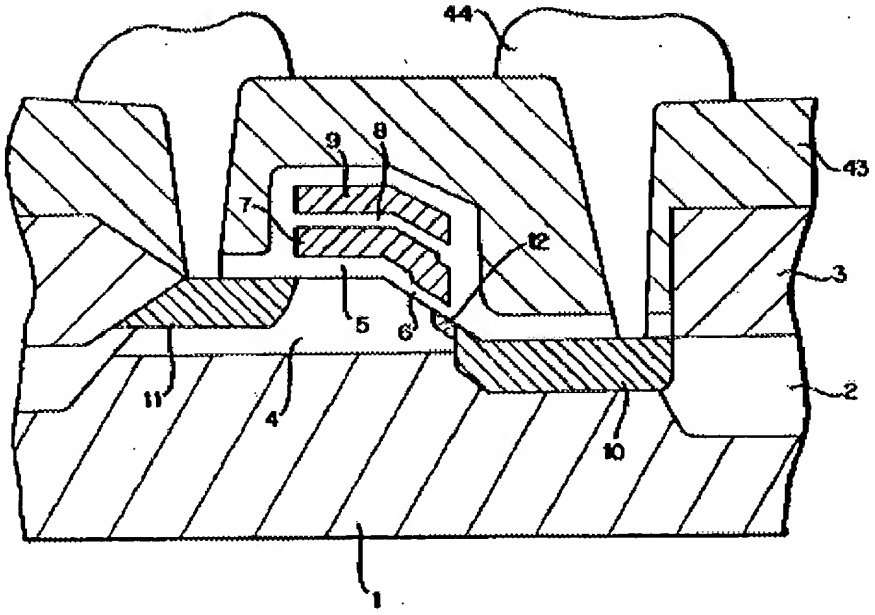
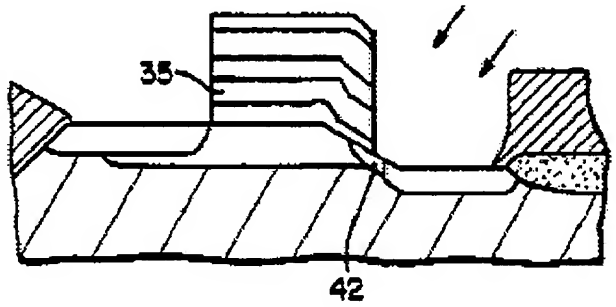


FIG. 13



Regarding claim 11, Matsushita further discloses that the implanting includes implanting the source and drain regions simultaneously (see figure 11 and column 17, lines 60-67 through column 18, lines 1-6).

Regarding claim 15, Matsushita also discloses that the implanting includes implanting the source and drain regions to a concentration of about 1.0E20 atoms/cm^3 (column 7, lines 50-53).

Regarding claim 18, Matsushita further discloses that the gate 7 is a floating gate and further includes forming a control gate 9 over the floating gate 7 (column 13, lines 53-55).

4. Claims 10, 13-14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kamiya et al. (U.S Pat. 4,794,433) of record.

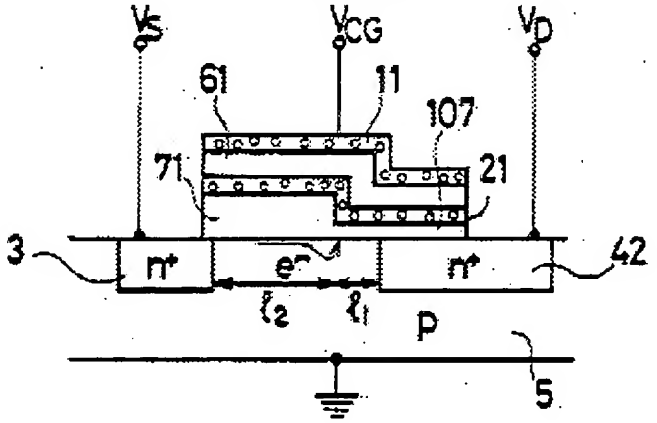
Regarding claims 10 and 13, Kamiya (figure 3) discloses a method of manufacturing a semiconductor device, comprising:

implanting source region 3 and drain region 42 having similar (N-type) doping profiles (column 2, lines 42-47) in a semiconductor substrate 5 (column 2, line 44) , thereby defining a channel region (l_2,l_1) extending from the source region 3 to the drain region 42;

locating a dielectric layer (71,107) over the source and drain regions (3,42), the dielectric layer (71,107) having a first thickness 71 and a second thickness 107, wherein the second thickness 107 of 80Å (column 4, lines 50-52) is substantially less than the first thickness 71 of 800Å (column 3, lines 14-15) and the second thickness 107 is partially located over the channel region (see figure 3 and column 2, lines 52-54); and

forming a gate 21 over the dielectric layer (71,107) (column 2, lines 66-67), wherein the second thickness 107 is located between an end of the gate 21 and one of the source and drain regions 42.

FIG. 3



Regarding claim 14, Kamiya (figure 3) further discloses that the locating includes an interface between first and second layers (71,107) of the dielectric layer by forming the second layer 107 on the channel region portion l_1 and the first layer 71 on the remaining channel region portion l_2 (column 2, lines 48-57).

Regarding claim 18, Kamiya (figure 3) further discloses that the gate 21 is a floating gate and further including forming a control gate 11 over the floating gate 21 (column 2, lines 66-68).

5. Claims 10 and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kachelmeier (U.S Pat. 5,741,737).

Regarding claim 10, Kachelmeier (figure 1) discloses a method of manufacturing a semiconductor device, comprising:

implanting source region 2 and drain region 3 (column 3, lines 45-55) having similar (N-type) doping profiles in a semiconductor substrate 1 (column 8, lines 1-3) , thereby defining a channel region (L) extending from the source region 2 to the drain region 3;

locating a dielectric layer (8,9) over the source and drain regions (2,3), the dielectric layer (8,9) having first thickness 8 and second thickness 9 wherein the second thickness 9 is substantially less than the first thickness 8 (column 2, lines 49-54) and the second thickness 9 is partially located over the channel region (see figure 1, column 2, lines 49-54); and

forming a gate 6 over the dielectric layer (8,9) (column 2, lines 37-38), wherein the second thickness 9 is located between an end of the gate 6 and one of the source and drain regions (2,3).

Regarding claims 12-13, Kachelmeier further discloses that the first thickness 8 ranges about 25 nm to about 50nm and the second thickness 9 ranges about 6nm and about 20nm as claimed (column 2, lines 49-54).

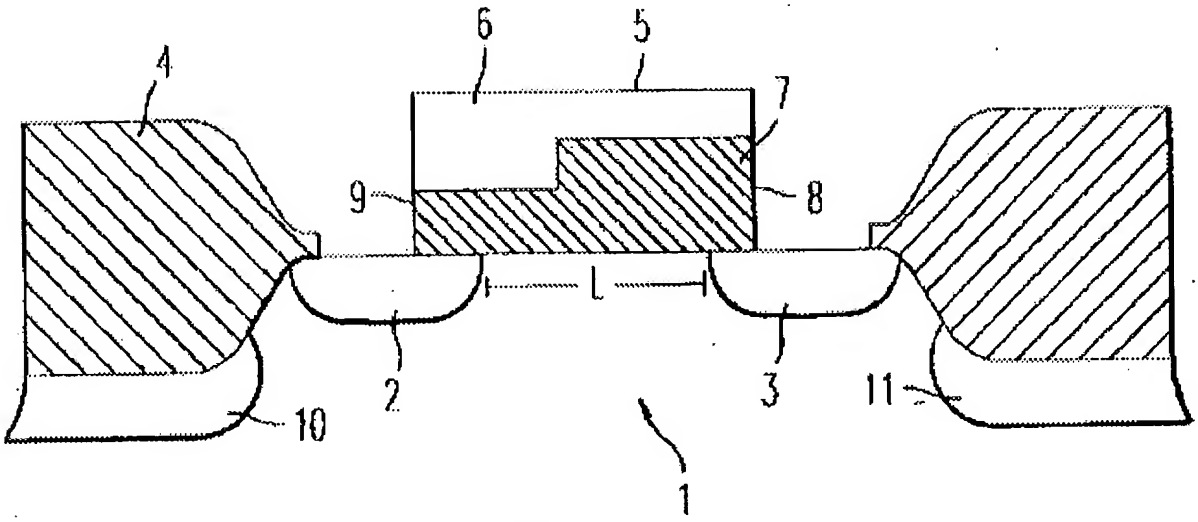


FIG. 1

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. (U.S Pat. 4,794,433) of record in view of Choi et al. (U.S Pat. 5,801,416).

Kamiya does not disclose that implanting includes a lightly doped region in each of the source and drain regions.

However, Choi (figure 3) discloses that implanting includes implanting a lightly doped region 48 in each of the source and drain regions (56,56a) (column 5, lines 50-53), wherein the end of a gate 45 and a second thickness 42 are located over one of the lightly doped regions 48 (see figure 3 and column 5, lines 40-41).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to include the step of implanting a lightly doped region in each of the source and drain regions of Kamiya, because as taught by Choi, such implanting a lightly doped region step is well known and commonly used in the art for preventing lower of the withstand voltage at the surface (column 2, lines 3-7).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. (U.S Pat. 4,794,433) of record in view of Choi et al. (U.S Pat. 5,801,416) as applied to claim 16 above and further in view of Matsushita (U.S Pat. 5,502,321).

Neither Kamiya nor Choi discloses the concentration of the lightly doped region in the range as claimed.

However, Matsushita (figure 13) teaches the forming of a lightly doped region 42 in the source/drain regions (column 18, lines 31-36), the lightly doped region 42 having the doped concentration of about 1.0E18 atoms/ cm^3 or less (column 18, lines 41-43).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the lightly doped region with the doped concentration in the range as set forth above because such doped concentration range of the lightly doped region would inhibit an increase in the leak current caused by the Zener phenomenon in the impurity diffusion layer immediately below the gate electrode with respect to the gate dielectric layer, as taught by Matsushita (column 18, lines 41-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
May 6, 2005.